MALT-32G-DAC

IP-Core. Digital-to-analog converter

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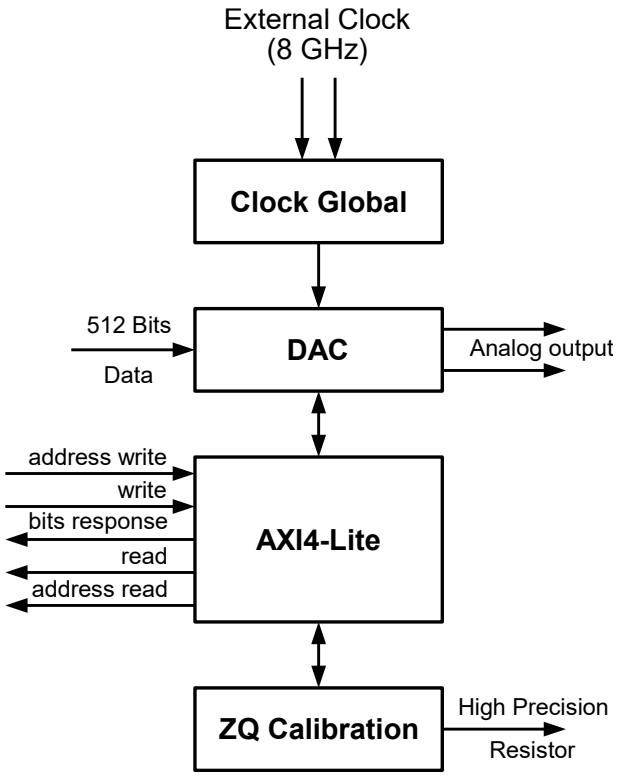

A high-speed RF DAC IP-core for direct generation of wideband analog signals. Based on the SST architecture, the block includes integrated tools for digital data preparation, generation of internal high-speed data streams, and clock adjustment. This enables data reception over a wide parallel bus and generation of a differential analog signal in real time at a high sampling rate. IP-core incorporates internal output path adjustment mechanisms, ensuring stable output parameters and matching with the external load. The digital part of the block receives the input data stream and contains the AXI-Lite control interface, which is necessary for configuring operating modes, running integrated calibration procedures, and monitoring status. This solution is designed for use in high-speed transmission paths, coherent optics systems, measurement equipment, and scientific instruments.

Technical specifications

IP-Core type:	Physical (HARD IP)
IP-Core status:	Silicon-proven in 2023
Technology, nm:	28
Resolution, bits:	8
Sampling rate, GSa/s:	24–32
Architecture:	SST-DAC
Analog output bandwidth, GHz:	16
Supply voltage, V:	0,9 (nom.)
Power dissipation, mW:	80-150 (32 GSa/s)
Output configuration:	differential with DC coupling
Output resistance, Ohms:	50 (per leg), 100 (diff.)
Output peak-to-peak voltage (diff.), mVpp:	14-900
DC offset, mV:	450
RMS aperture jitter, fs:	60
Macro area, mm^2:	0,033
Delivery terms:	Ready for delivery

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Applications

- Transmission paths for coherent optical systems, including DP-QPSK and 16-QAM;
- Transmission paths for data center interconnect (DCI) systems, including 100G/200G/800G Ethernet;

- High-speed arbitrary waveform generators and other test and measurement equipment;
- Measurement and research systems, including quantum computing and spectroscopy;
- Specialized SoCs for arbitrary waveform generation of high-frequency signals.

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