MALT-DDR-PHY

IP-Core. DDR4 SDRAM physical layer

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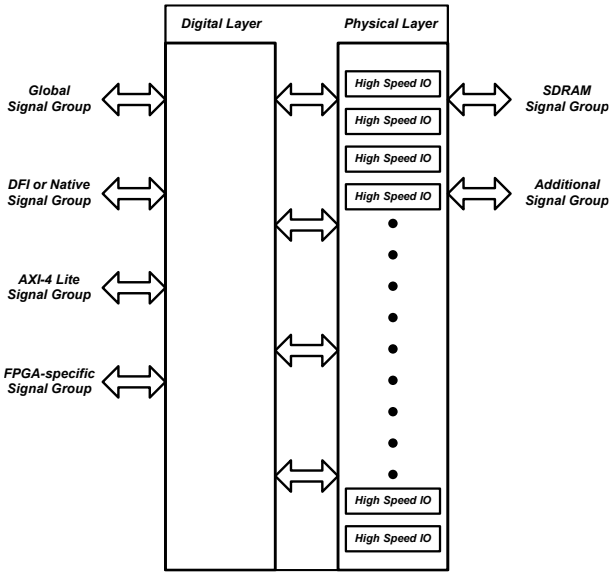

The IP-core is designed for interfacing with synchronous dynamic random-access memory (SDRAM). All control logic is located on an external controller connected via a standard DFI interface. This architecture provides maximum flexibility. A custom optimized controller can be used, while the IP-core guarantees signal integrity and compliance with the JESD79-4C (DDR4) specification. The digital portion of the core contains the AXI-4 Lite configuration interface for register configuration. The integrated data link controller enables basic calibration functions, generates test sequences for external SDRAM memory, and accesses MR registers. A controller-independent training mode for the physical layer interface is used to align write and read signals. Data transfer efficiency is ensured by an integrated clocking circuit in the form of a high-speed PLL block. The solution is designed for use in servers, special processors and accelerators for high-performance computing, as well as for systems-on-chip equipped with their own DDR4 SDRAM controllers.

Technical specifications

IP-Core type:	Physical (HARD IP)
IP-Core status:	Silicon-proven in 2023
Technology, nm:	28
SDRAM DDR4 standard JEDEC, -:	JESD79-4C (3200 MT/s)
SDRAM DDR4 speed, MT/c:	1600, 1866, 2133, 2400, 2666, 2933, 3200
Data Bus, bits:	64
Type of oxide layer of input-output transistors (OD2), V:	1.8
Packaging method, -:	Flip Chip support
Supply voltage, V:	0.9 & 1.2;
Output driver resistance, Ohms:	34, 40, 48, 60, 80, 120, 240;
Receiver ODT, Ohms:	34, 40, 48, 60, 80, 120, 240;
Interface, -:	– DDR PHY Interface (DFI) – Native
Power dissipation, mW:	4000
Macro area, mm^2:	7,1
Delivery terms:	Ready for delivery

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Applications

- High-performance computing using specialized processors and accelerators (AI/ML, GPU, DSP);
- Buffering packets of network processors and switches in DDR4 memory with minimal latency;
- SoCs equipped with their own DDR4 SDRAM controllers optimized for specific algorithms.